REMARKS

This Response seeks to place this application in condition for allowance. All of the Examiner's rejections have been addressed below. Some of the pending claims have been amended to improve clarity, antecedence, and/or to more particularly point out the subject matter. New dependent claims 29-37 have been added to more fully protect Applicants' invention. No new matter has been added.

Office Action

In the non-final Office Action dated February 22, 2002 (hereinafter, "OFFICE ACTION"), the Examiner rejected claims 1-24, and 26-27 under 35 U.S.C. §102 as being anticipated by U.S. Patent No. 6,329,694 to Lee et al. (hereinafter, "Lee"). Dependent claim 28 was rejected under 35 U.S.C. §103 as being unpatentable over Lee.

Applicants submit that independent claims 1, 12, and 23 are not rendered obvious or anticipated by Lee. It should be noted that, although not separately addressed herein, dependent claims 2-11, 13-22, 24, and 26-28 incorporate limitations that present patentable subject matter in their own right. In short, these limitations are also not rendered obvious or anticipated by Lee. However, in an attempt to present a more concise response to the OFFICE ACTION, only certain limitations or elements of independent claims 1, 12 and 23 are discussed below. No inference or conclusion of any kind should be drawn from the absence of comments pertaining to other limitations or elements, whether those limitations or elements are contained in independent or dependent claims.

Claim 1 is Not Anticipated By Lee

Applicants respectfully submit that independent claim 1 (in it's amended or pre-

amendment form) is not anticipated by Lee. Claim 1 is directed toward an integrated circuit and recites (as amended), in part:

> a **conductive pad** to receive an input signal from an external signal line;
> a **first doped region** of first a conductivity type disposed in a semiconductor substrate of a second conductivity type, wherein the first doped region is underlying and surrounding the conductive pad;
> (emphasis added)

Lee, in contrast to claim 1, does not disclose, for example, a first doped region underlying and surrounding a conductive pad. Rather, in Lee, the source region 54 of the NMOS structure and the source region 63 of the PMOS structure are described as being "connected to an input/output pad (I/O pad)." (See, Lee at Col. 5, lines 42-43). However, in Lee, the position of the I/O pad is not shown relative to n-well 61 and "p+ pick-up 65" . Contrary to the Examiner's remark in the OFFICE ACTION (see page 2, item 1), n-well 61 is not shown or described as "underlying and surrounding the conductive pad."

Thus, for at least these reasons, Lee does not anticipate independent claim 1 or claims 2-11 which depend therefrom.

Claim 12 is Not Anticipated By Lee

Applicants have amended claim 12 to more particularly point out the subject matter. Applicants respectfully submit that Independent claim 12 (in its amended or pre-amendment form) is not anticipated by Lee. Claim 12 is directed to a bond pad for an integrated circuit device. Claim 12 (as amended) recites in part:

> a **conductive region** of the first conductivity type disposed in the doped region, wherein the conductive region is underlying the conductive bonding layer and wherein the conductive region includes a surface area that is at least substantially equal to the surface area of the conductive bonding layer;

(emphasis added)

At the very least, Lee does not disclose, for example, a bond pad including "a conductive region . . . disposed in the doped region [and] . . . having a surface area at least substantially equal to the surface area of the conductive bonding layer". In this regard, Applicants note the Examiner's remarks regarding: the conductive bonding layer, i.e., "... the bond pad comprising conductive layers 63-65"; and the conductive region, i.e., "a conductive region 65... having a surface area at least substantially equal to the surface area of the conductive bonding layer". Applicants submit that in Lee, "p+ pickup 65" does not have a surface area that is at least substantially equal to the combined surface area of source 63, drain 64 and "p+ pick-up 65" (see page 3 of the OFFICE ACTION). Rather, p+ pickup 65, includes a surface area that is **much** less than the combined surface areas of source 63, drain 64 and "p+ pick-up 65". Thus, for at least these reasons, Lee does not anticipate independent claim 12 or claims 13-22 which depend therefrom.

Notwithstanding the aforementioned remarks, Applicants have amended claim 12 to more particularly point out the subject matter. In this regard, claim 12 recites in part that "...the conductive region is underlying the conductive bonding layer".

Claim 23 is Not Anticipated By Lee

Applicants respectfully submit that Independent claim 23 (in its amended or pre-amended form) is not anticipated by Lee. Claim 23 is directed to a transistor layout and, as amended, recites in part:

> a **drain** region having a first conductivity type doping, wherein the drain region is formed in a semiconductor substrate region having a second conductivity type doping, the drain region being electrically coupled to the bond pad;
> a **source** region including a second conductivity type doping;

(emphasis added)

Lee, in contrast to claim 23, does not disclose, for example, "a drain region having a first conductivity type doping... and a source region including a second conductivity type doping". Instead, Lee in Fig. 14, shows a transistor cross-section view of NMOS and PMOS transistors each having source and drain regions of the same conductivity type exclusively[1]. The transistor cross-section shown in Fig. 14 of Lee illustrates a conventional NMOS transistor having n+ type source and drain regions and a conventional PMOS transistor having p+ type source and drain regions.

Thus, for at least these reasons, Lee does not anticipate independent claim 23 or claims 24, 26 and 27 which depend therefrom.

[1] These comments are in no way intended to exclude claim 23 from reading on the implementation where the source region includes both p-type and n-type doping (e.g., see claim 29, i.e. "wherein the source region includes the first conductivity type doping"). Indeed, as is disclosed in the specification of the instant application, in one embodiment, transistor 600 (see Fig. 6) is an NMOS transistor having (n-type doped) source region 610 which "structurally integrates" a portion of (p-type doped) conductive tap region 640 as "a homogeneous conductive region" (e.g., see page 20, lines 14-17, and page 19, line 14 to page 20, line 10).

Conclusion

Applicants request reconsideration of the instant application in view of the foregoing remarks. Applicants submit that the pending claims present patentable subject matter. Accordingly, allowance of all of the claims is respectfully requested.

The Examiner is invited to contact the undersigned if a telephone call could help resolve any remaining issues

Respectfully submitted,

Date: May 22, 2002

Jose G. Moniz
Reg. No. 50,192
650-947-5336

Exhibit A – Version With Markings to Show Changes Made to The Claims

1. **(Twice Amended)** An integrated circuit device comprising:

a conductive pad to receive an input signal from an external signal line;

a first doped region of a first conductivity type disposed in a semiconductor substrate of a second conductivity type, wherein the first doped region is underlying and surrounding the conductive pad;

a conductive region of the first conductivity type disposed in the first doped region;

a first tap region spaced apart from and surrounding a substantial portion of the first doped region, wherein the first tap region is electrically coupled to a first supply voltage;

an output driver transistor having a drain region and a source region, wherein the drain region is electrically coupled to the conductive pad; and

a second tap region surrounding the output driver transistor, wherein the second tap region is electrically and physically coupled to a second supply voltage and the source region.

5. **(Twice Amended)** The integrated circuit device of claim 1 wherein [the] a doping concentration of the first doped region is less than [the] a doping concentration of the conductive region.

6. **(Amended)** The integrated circuit device of claim 1 wherein the first tap region is a [third] second doped region and the second tap region is a [fourth] third doped region.

7. **(Twice Amended)** The integrated circuit device of claim 6 wherein the [third] second doped region is of an opposite conductivity type than the first doped region.

8. **(Twice Amended)** The integrated circuit device of claim 6 wherein the [fourth] third doped region is a P type doped region and the output driver transistor is an NMOS type transistor.

9. **(Amended)** The integrated circuit device of claim 1 [wherein a portion of the first] further including a tap region portion that is spaced apart from and surrounding the first doped region, wherein the tap region portion is decoupled from the first supply voltage to provide a predetermined [equivalent series] resistance between the first doped region and the first supply voltage.

10. **(Twice Amended)** The integrated circuit device of claim 1 [5] wherein a portion of the [first] second tap region is integrated into the source [substantially surrounds the first doped] region.

12. **(Twice Amended)** A bond pad for an integrated circuit device, the bond pad comprising:

a conductive bonding layer;

a [first] doped region of a first conductivity type formed in a semiconductor substrate of a second conductivity type, wherein the doped region is underlying and surrounding the conductive bonding layer;

a conductive region of the first conductivity type disposed in the [first] doped region, wherein the conductive region is underlying the conductive bonding layer and wherein the conductive region [having] includes a surface area at least substantially equal to [the] a surface area of the conductive bonding layer; and

a conductive tap region spaced apart from and surrounding at least a portion of the [first] doped region, wherein a portion of the conductive tap region is electrically coupled to a supply voltage.

14. **(Twice Amended)** The bond pad of claim 12 wherein the doping concentration of the [first] doped region is less than the doping concentration of the conductive region.

15. **(Amended)** The bond pad of claim 12 wherein the conductive tap region is [a third] doped [region and is] to be of an opposite conductivity type than the first doped region.

16. **(Amended)** The bond pad of claim 12 [wherein a portion of the] further including a

conductive tap region portion that is spaced apart from and surrounding the doped region, wherein the conductive tap region portion is decoupled from the supply voltage to provide a predetermined [equivalent series] resistance between the doped region and the supply voltage.

18. **(Twice Amended)** The bond pad of claim 17 wherein the conductive tap region completely [substantially] surrounds the doped region.

22. **(Amended)** The bond pad of claim 21 wherein the conductive tap region is a [an] doped layer positioned beneath the conductive region.

23. **(Twice Amended)** A transistor layout for an integrated circuit device having a bond pad, the transistor layout comprising:

a drain region [of] having a first conductivity type doping, wherein the drain region is formed in a semiconductor substrate region having a [of] second conductivity type doping, the drain region being electrically coupled to the bond pad;

a source region [of] including a second conductivity type doping; and

a conductive tap region spaced proximal to and surrounding the drain region, wherein the conductive tap region is electrically coupled to a supply voltage and electrically and physically coupled to the source region.

24. **(Amended)** The transistor layout of claim 23 wherein the supply voltage is [coupled to] a ground voltage.